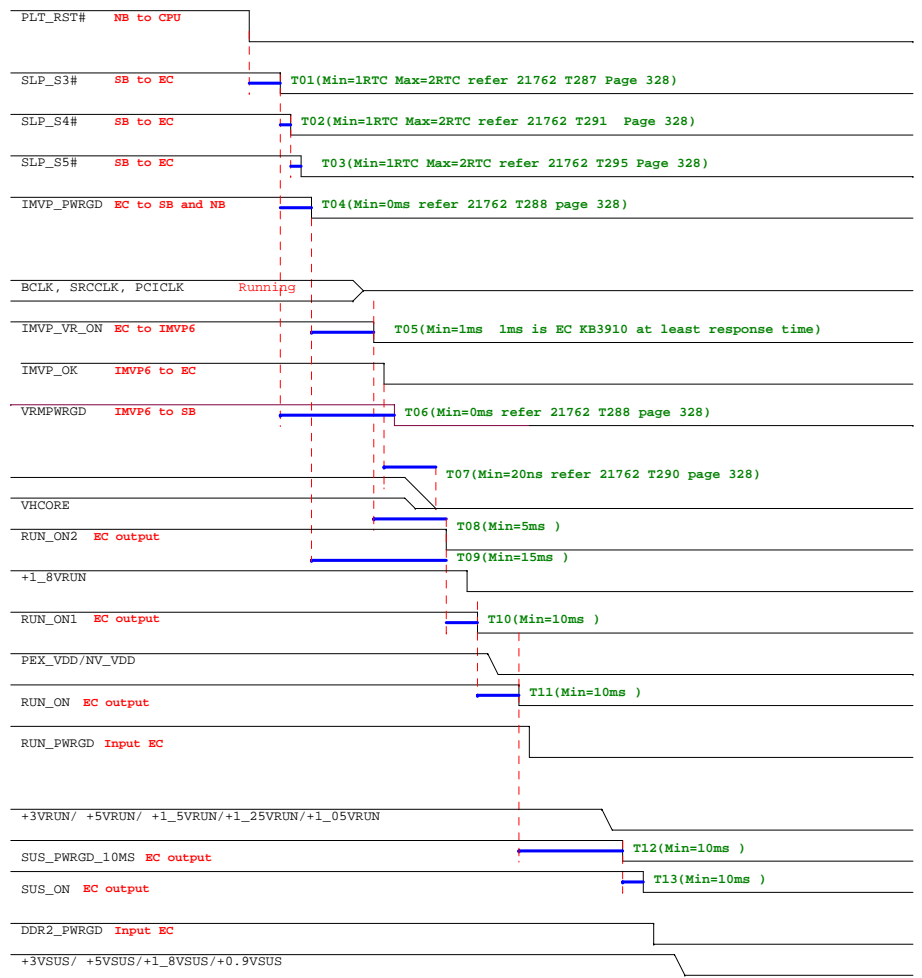
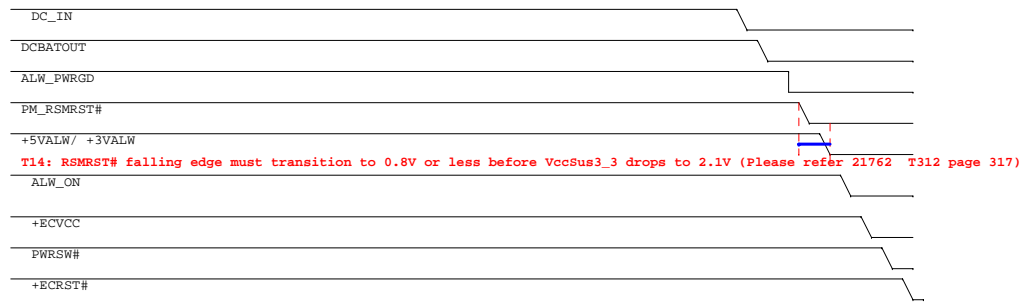


11/17:
 Check if it's ok to use IMVP_OK to replace
 EC_CLK_EN#, it can save one inverter



(S5 to G3)



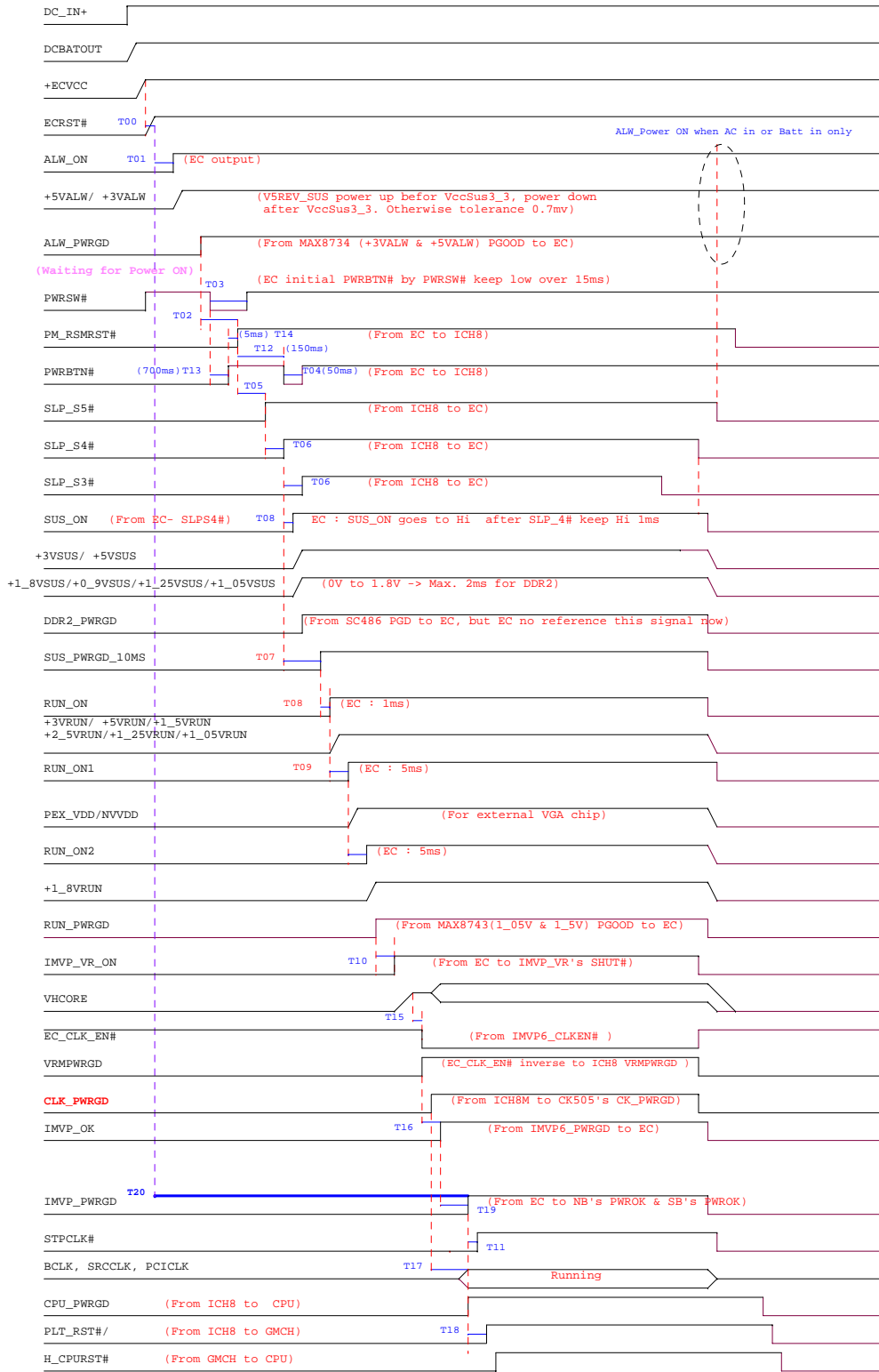
T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	T12	T13	T14
1 - 2	1 - 2	1 - 2	Min.	Min.	Min.	Min.	Min.	Min.	Min.	Min.	Min.	Min.	*1
RTCLK	RTCLK	RTCLK	0ms	15ms	0ms	20ns	5ms	15ms	10ms	10ms	10ms	10ms	

*1 RSMRST# falling edge must transition to 0.8V or less before VccSus3_3 drops to 2.1V

MS90 Power On Sequence Timing

Version : 0.5

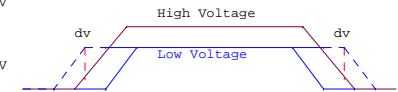
NOTE : (EC KB3910 Min. response time is 1ms)



- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 19513 Page 286 of t200 timing) --> Check(t200 did not say so)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 10ms (Refer t204 of Intel 20271 page 304)
- T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms (Refer to t231 of Intel 20271 page 306)
- T06 : Please reference t233/t234 of Intel 20271 page 306 => Checking
- T07 : For MS01 current SPEC Min. is 25 ms.--> Checking
- T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- T09 : EC delay 5ms
- T10 : Please refer to t214 of Intel 20271 page 304
- T11 : Please refer to t215 of Intel 20217 page 304
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 150ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing) -->Checking
- T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- When Powered on, the DDR2 1.8V rail must ramp up from 0 to 1.8V within 2ms. (Refer to Intel 20517 page 44)
- ~~IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)~~
- In NV4X power sequence : NV_VDD,VRAMPVDD,PEX_VDD and VRAM_TERM can ramping up anytime after +3VRUN starts ramping up.(Please refer to DG-00969_v05c Page 50 for NV4x GPU power sequencing description)
- T15 : Refer ISL6262A Spec no mention.
- T16 : Refer ISL6262A Spec page3 PGOOD DELAY.
- T17 : Refer to ICS9LPR501VGLFT CK505 Spec.
- T18 : The ICH8 drives PLTRST# inactive a minimum of 1ms after both PWROK and VRMPWRGD are driven high. (Refer to Intel 20217)
- CPUPWRGD is an output signal that represents a logical AND of the ICH8's PWROK and VRMPWRGD signals.
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV) SPEC please refer to Intel 20517 16.7 GMCH/ICH8M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1_5VRUN -> +1_05VRUN, dt:0.7mV
- +3_3VRUN -> +2_5VRUN, dt:0.3mV
- +3_3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV
- Check +1_05VRUN and VCC1_5_A[25] => Refer Intel 20517 page 438



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
R/C delay (47K/0.1uF)	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1-2 RTCCCLK (Checking) 25 ms	Min. 25 ms	1ms	Min. 5ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 150ms	Min. 700ms	Min. 5ms	TBD	Min : 5.5ms Max : 8.1ms	Min : 1.8ms	Min : 1ms	Min : 99ms	Min : 1s	

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Change List

[V0.2]

1. STPCLK#, CPUSLP#, STP_CPU#/PCI# --> STPCLK#
2. Correct T11 from "IMVP_OK to STPCLK#" --> "IMVP_PWRGD to STPCLK#" (Refer ICH8M EDS T215)
3. Correct down side table T09 from 10ms to 5ms.
4. Correct T18 from "IMVP_OK to PLT_RST#" --> "IMVP_PWRGD to PLT_RST#" (Refer ICH8M ESD)
5. Correct H_CPURST to H_CPURST#
6. Add ICH8M's CK_PWRGD to enable CK505's PWRGD
7. Update CLK_EN# to EC_CLK_EN#

[V0.3]

1. Correct: PWRSW# is driven by EC, not ICH8M
2. Add note: Check if it's ok to use IMVP_OK to replace EC_CLK_EN#, it can save one inverter

[V0.4]

1. Add power off sequence

[V0.5]

1. Correct T12 from min:400ms to 150ms
This modify already phase in MS90-DVT stage.

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